EE/CS 120 Logic Design Course Objectives:

1. Able to perform the conversion among different number systems; Familiar with baisc logic gates -- AND, OR & NOT, XOR, XNOR; Independently or work in team to build simple logic circuits using basic.
2. Understand Boolean algebra and basic properties of Boolean algebra; able to simplify simple Boolean functions by using the basic Boolean properties.
3. Able to design simple combinational logics using baisc gates. Able to optimize simple logic using Karnaugh maps, understand "don't care".
4. Familiar with basic sequential logic components: SR Latch, D Flip-Flop and their usage and able to analyze sequential logic circuits.
5. Understand finite state machines (FSM) concepte and work in team to do sequence circuit design based FSM and state table using D-FFs.
6. Familiar with basic combinational and sequential components used in the typical datapath designs: Register, Adders, Shifters, Comparators; Counters, Multiplier, Arithmetic-Logic Units (ALUs), RAM. Able to do simple register-transfer level (RTL) design.
7. Able to understand and use one high-level hardware description languages (VHDL or Veriliog) to design combinational or sequential circuits.
8. Understand that the design process for today's billion-transistor digital systems becomes a more programming based process than before and programming skills are important.