Homework 2

6.3. (Section 6.2) Perform two-level logic size optimization for the function F(a, b, c) = a + a'b'c + a'c using a K-map. Express the answer as sum-of-products.

6.4. (Section 6.2) Perform two-level logic size optimization for the function F(a, b, c, d) = a'bc' + abc'd' + abd using a K-map. Express the answer as sum-of-products.

2.36. (Section 2.6) Create the Boolean equations for the digital circuit in Figure 2.38.

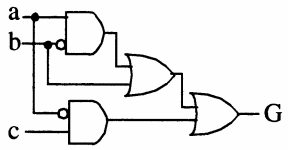


Figure 2.38: Combinational circuit *G*.

2.38. (Section 2.6) Create a truth table for the circuit in Figure 2.38.

2.44. (Section 2.7) Using the combinational design process of Table 2.3, create a circuit for unlocking one of 8 doors capturing the circuit behavior using Boolean equations. Each door is unlocked by setting the door's unlock input to 1. Door 0's input is named U0, door l's input is named U1, and so on. We specify which door to unlock using a 3-bit input value D. So D=000 unlocks door 0, D=001 unlocks door 1, etc.

2.47. (Section 2.8) Determine whether the two circuits in Figure 2.41 are equivalent circuits using algebraic manipulation, and then using truth tables.

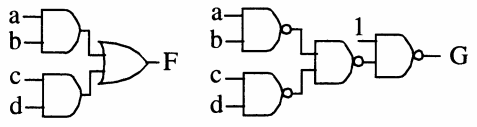
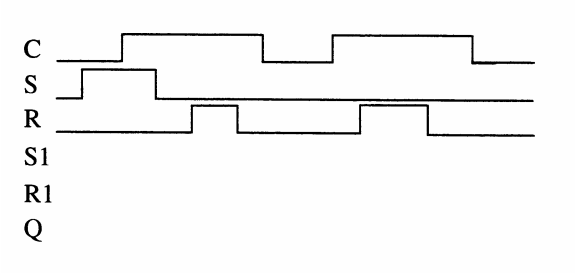


Figure 2.41: Combinational circuits *F* and *G*.

2.57. (Section 2.9) Design a 3x8 decoder.

3.6. (Section 3.2) Trace the behavior of an SR latch for the following situation: Q, S and R are 0 and have been for a long time, then S changes to 1 and stays there for a long time, then S changes back to 0. Using a timing diagram, show the values that appear on every wire for every change on a wire. Assume logic gates have a tiny but non-zero delay.

3.8. (Section 3.2) Trace the behavior of a level-sensitive SR latch for the following input pattern. Complete the timing diagram, assuming logic gates have a tiny but non-zero delay.



3.10. (Section 3.2) Trace the behavior of an edge-triggered D flip-flop using the master-slave design for the following input pattern. Complete the timing diagram, assuming logic gates have a tiny but non-zero delay.